CLAIM AMENDMENTS

1. (Currently Amended) An apparatus, comprising:

a first block to process a first type of frame in a video bitstream using a first error resilience technique; and

a second block to process a second type of frame in the video bitstream using a second error resilience technique, wherein the first error resilience technique is different from the second error resilience technique, the second error resilience technique to replace a bit pattern for the second type of frame with a shorter bit pattern.

2. (Previously Amended) The apparatus of claim 1, wherein the first block further processes a third type of frame.

3. (Original) The apparatus of claim 1, wherein the second block comprises a resynchronization marking block.

4. (Original) The apparatus of claim 3, wherein the second block comprises a variable length coder block.

5. (Original) The apparatus of claim 1, wherein the first block applies resynchronization markers to the video bitstream at a first interval and the second block applies resynchronization markers to the video bitstream at a second interval, wherein the second interval is longer than the first interval.

6. (Original) The apparatus of claim 1, wherein the second block inserts fewer error resilience bits in the video bitstream than the first block.

7. (Original) The apparatus of claim 1, further comprising a third block to process the P-type frame using a first error concealment technique.

8. (Previously Amended) The apparatus of claim 7, further comprising a fourth block to process the second type of frame using a second error concealment technique, wherein the first error concealment technique is different from the second error concealment technique.

9. (Original) The apparatus of claim 1, wherein the first block comprises:

a data partitioning block having an input terminal and an output terminal;

a reversible variable length coder block having an input terminal and an output terminal, wherein the output terminal of the data partitioning block is coupled to the input terminal of the reversible variable length code block;

a header extension code block having an input terminal and an output terminal, wherein the output terminal of the reversible variable length code block is coupled to the input terminal of the header extension code block; and

a resynchronization marker block having an input terminal and an output terminal, wherein the output terminal of the header extension code block is coupled to the input terminal of the resynchronization marker block.

10. (Currently Amended) An article comprising one or more machine-readable storage media containing instructions that when executed enables a processor to:

receive a video stream having at least a first type of frame and a second type of frame; and

process the first type of frame using a first error resilience technique and the second type of frame using a second error resilience technique, wherein the first error resilience technique comprises applying resynchronization markers to the video stream at a selected interval and the second error resilience technique comprises applying resynchronization markers at an interval different from the selected interval such that the second error resilience technique replaces a bit pattern for the second type of frame with a bit pattern of shorter length.

11. (Original) The article of claim 10, wherein the instructions when executed enable the processor to process a P-type frame using the first error resilience technique.

12. (Original) The article of claim 11, wherein the instructions when executed enable the processor to process a B-type frame using the second error resilience technique.

13. (Original) The article of claim 12, wherein the instructions when executed enable the processor to process the B-type frame using a simpler error resilience technique than the P-type frame.

14. (Original) The article of claim 13, wherein the instructions when executed enable the processor to insert resynchronization markers in the video stream at a first pre-selected interval for the B-type frame and at a second pre-selected interval for the P-type frame, wherein the first pre-selected interval is longer than the second pre-selected interval.

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15. (Original) The article of claim 10, wherein the instructions when executed enable the processor to process the first type of frame using a first error concealment technique and the second type of frame using a second error concealment technique, wherein the first error concealment technique is different from the second error concealment technique.

16. (Original) The article of claim 10, wherein the instructions when executed enable the processor to insert fewer error resilience bits into the video stream for the B-type frame than for the P-type frame.

17. (Original) The article of claim 10, wherein the instructions when executed enable the processor to perform variable length coding on the B-type frame.

18. (Original) The article of claim 10, wherein the instructions when executed enable the processor to apply resynchronization markers to the video for the B-type frame.

19. (Currently Amended) An apparatus, comprising:

a first block to process a first type of frame in an encoded bitstream using a first error concealment technique; and

a second block to process a second type of frame in the encoded video bitstream using a second error concealment technique, wherein the first error concealment technique is different from the second concealment technique <u>such that the second error concealment technique copies data lost from a previous second type of frame</u>.

20. (Original) The apparatus of claim 19, wherein the second block comprises a variable length decoder block.

21. (Original) The apparatus of claim 19, wherein the second error concealment technique comprises performing a block copy.

22. (Currently Amended) A method comprising:

receiving a video stream;

performing error resilience on a first type of frame within the video stream using a first technique; and

performing error resilience on a second type of frame within the video stream using a second technique, wherein the first technique is different from the second technique such that the second error resilience technique replaces a bit pattern for the second type of frame with a shorter length bit pattern.

23. (Original) The method of claim 22, further comprising performing error resilience on an I-type frame.

24. (Original) The method of claim 22, wherein the first technique comprises applying resynchronization markers to the video bitstream at a first interval and the second technique comprises applying resynchronization markers at a second interval, wherein the second interval is longer than the first interval.

25. (Original) The method of claim 22, wherein the second technique inserts fewer error resilience bits in the video bitstream than the first error resilience technique.

26. (Currently Amended) The method of claim 22, further including performing error concealment on the [[P-type]] first type of frame using a first technique and performing error concealment on the [[B-type]] second type of frame using a second technique, wherein the first technique is different from the second technique.

27. (Currently Amended) An apparatus, comprising:

a first block to perform error concealment on an encoded video signal and provide an output signal;

a second block to determine at least one channel characteristic; and

a third block to perform error resilience on the output signal based on the at least one channel characteristic and provide a modified video signal, wherein the third block performs error resilience on a first type of frame using a first technique and on a second type of frame

using a second technique such that the second error resilience technique to replace a bit pattern for the second type of frame with a shorter length bit pattern.

28. (Original) The apparatus of claim 27, further comprising at least of a block to transmit the modified signal and to store the modified signal to a storage device.

29. (Canceled)

30. (Original) The apparatus of claim 27, wherein the first block performs error concealment on a P-type frame using a first technique and on a B-type frame using a second technique, wherein the first technique is different from the second technique.

31. (Previously Presented) The apparatus of claim 1 wherein said first type of frame is a P-type frame and said second type of frame is a B-type frame.

32. (Previously Presented) The apparatus of claim 2 wherein said third type of frame is an I-type frame.

33. (Previously Presented) The apparatus of claim 19, wherein said first type of frame is a P-type frame and said second type is a B-type frame.